Description

The PJ9501 Series is a low-dropout (LDO) voltage regulators with enable function that operates from 2V to 7V. It provides up to 500mA of output current and offers low-power operation in miniaturized packaging. The features of low quiescent current as low as 1μA and almost zero disable current is ideal for powering the battery equipment to a longer service life.The other features include current limit function, over temperature protection and output discharge function.

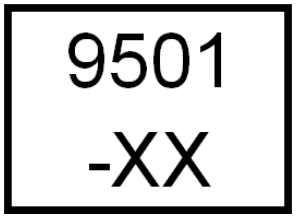
Features

- Ultra Fast Response in Line/Load Transient
- Maximum Output Current: 500mA
- Low Dropout : 230mV @ 200mA(3.3V)
- Wide Operating Voltage Ranges : 2V to 7V
- Over-Temperature Protection
- Current Limiting Protection
- Thermal Shutdown Protection

Applications

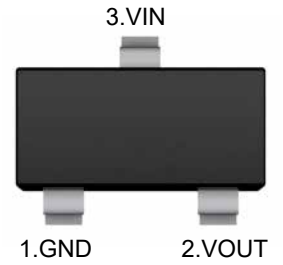
- Battery-Powered Equipment
- Ultra Low Power Microcontrollers
- Notebook Computers

Marking Code

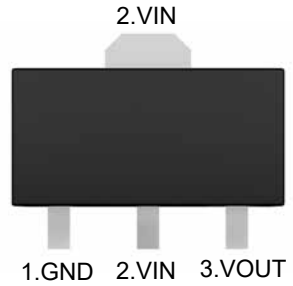


XX:Output Voltage
e.g. 3.0:3.0V 3.3:3.3V

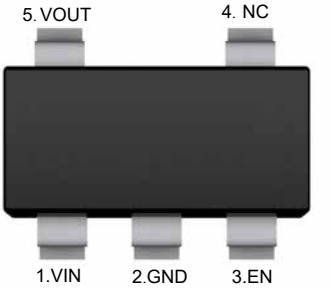
SOT-23-3



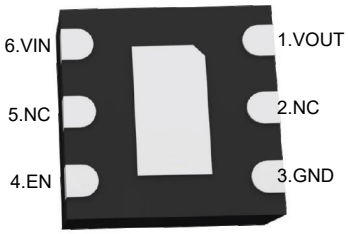
SOT-89



SOT-23-5



DFN2x2C-6L



Functional Pin Description

Pin Name	Pin Function
EN	Chip Enable (Active High). Note that this pin is high impedance
NC	NO Connected
GND	Ground
VOUT	Output Voltage
VIN	Power Input Voltage

Ordering Information

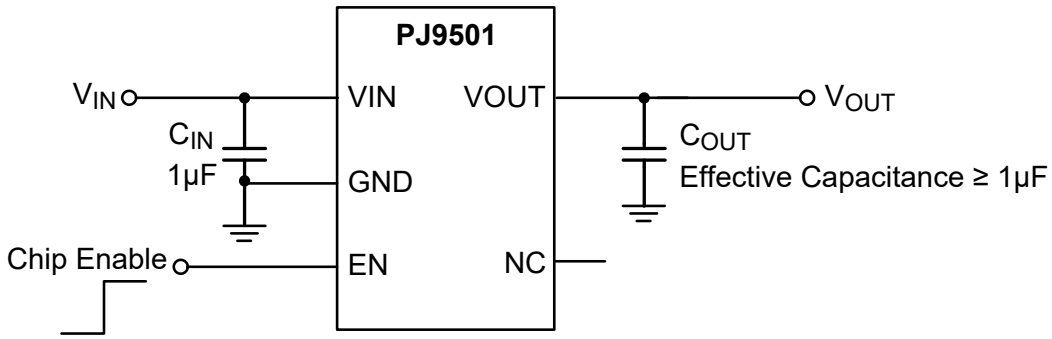
PJ9501- □□□□

Package Type
SC : SOT-23-3
SE : SOT-23-5
SQ : SOT-89
DFC : DFN2x2C-6L

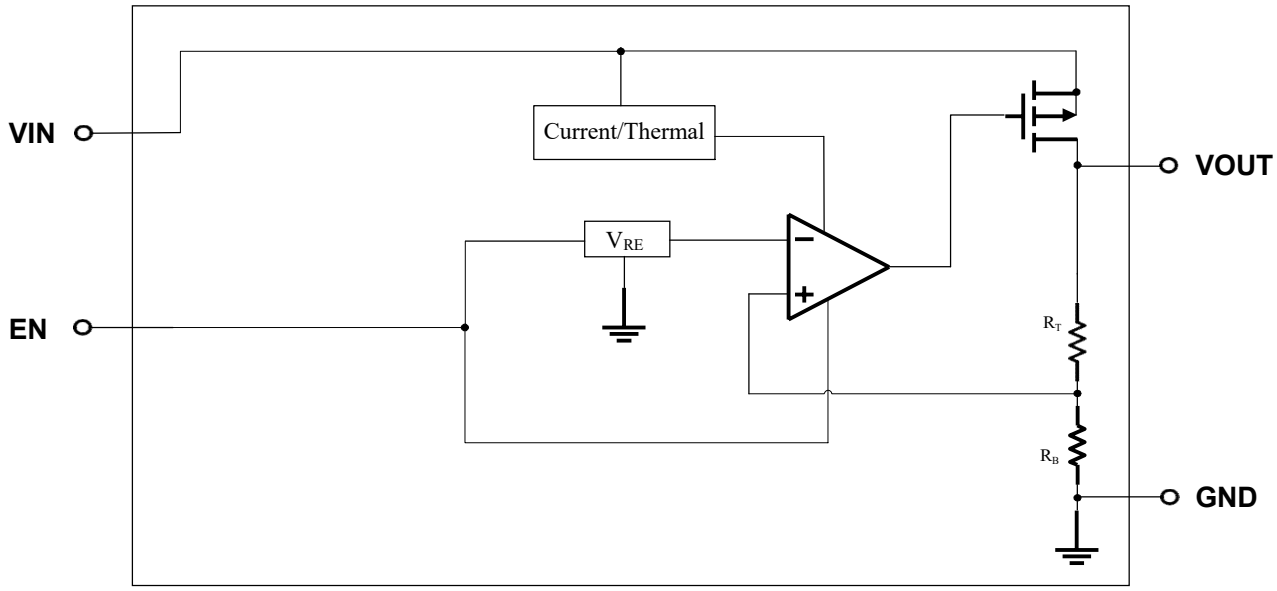
12 : 1.2V 15 : 1.5V 18 : 1.8V
25 : 2.5V 28 : 2.8V 30 : 3.0V
33 : 3.3V 36 : 3.6V

Output current tap
M : 500mA

Typical Application Circuit



Function Block Diagram



Absolute Maximum Ratings Note1

Ratings at 25℃ ambient temperature unless otherwise specified.

Parameter		Value	Unit
VIN,VEN to GND Voltage		-0.3 ~ +9	V
VOUT to VIN Voltage		-0.3~VIN+0.3	V
Power Dissipation	SOT-89	500	mW
	SOT-23-3	450	mW
	SOT-23-5	450	mW
	DFN2x2C-6L	560	mW
Thermal Resistance,Junction-to-Ambient	SOT-89	200	°C/W
	SOT-23-3	220	°C/W
	SOT-23-5	220	°C/W
	DFN2x2C-6L	180	°C/W
Operating Ambient Temperature		-40~ +85	°C
Junction temperature		260	°C
Storage temperature range		-50 ~ +125	°C
ESD(HBM)		4	KV
ESD(CDM)		200	V

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

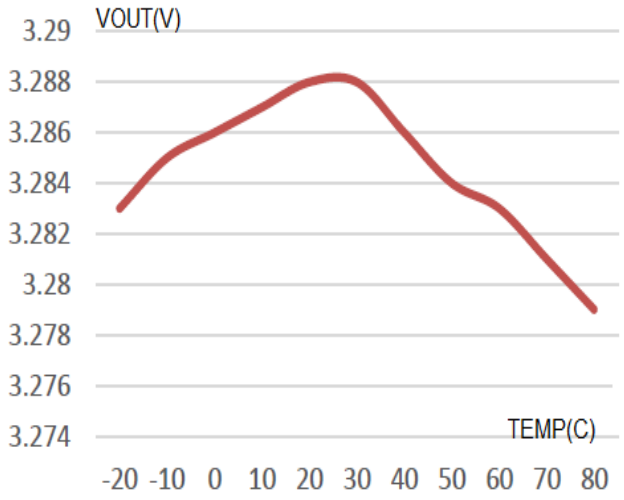
Electrical Characteristics

(V_{IN}=V_{OUT}+1, EN=V_{IN}, C_{IN}=1μF, C_{OUT}=1μF, T_A=25℃ , unless otherwise noted.)

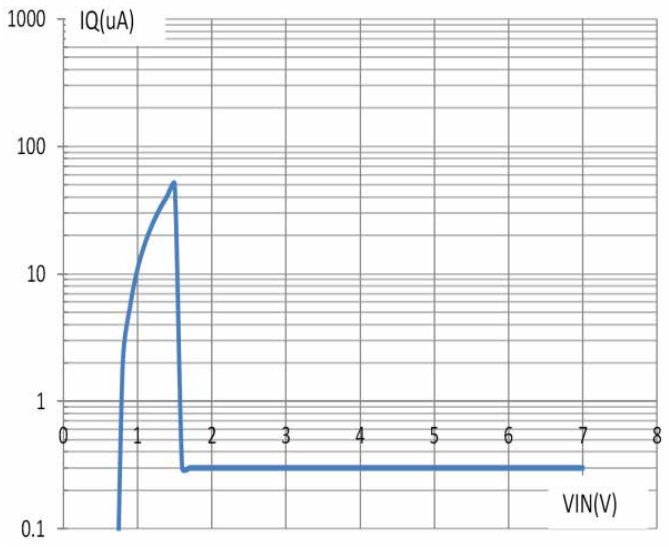
Parameter		Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Input Voltage		V_{IN}			2	--	7	V
Output Voltage Accuracy		ΔV_{OUT}	I_{OUT}=1mA		-1.5	--	+1.5	%
Quiescent Current		I_Q	V_{IN}>V_{OUT},EN=V_{IN} I_{OUT}=0mA		--	1	3	μA
Dropout Voltage Note1		V_{DROP}	I_{OUT}=200mA	1.2V≤V_{OUT}<1.5V	--	1.1	1.2	V
			I_{OUT}=200mA	1.5V≤V_{OUT}<1.8V	--	1	1.1	
			I_{OUT}=200mA	1.8V≤V_{OUT}<2.5V	--	0.4	0.5	
			I_{OUT}=200mA	2.5V≤V_{OUT}<2.8V	--	0.26	0.4	
			I_{OUT}=200mA	2.8V≤V_{OUT}<3.3V	--	0.26	0.35	
			I_{OUT}=200mA	V_{OUT}≥3.3V	--	0.23	0.3	
Dropout Voltage Note1		V_{DROP}	I_{OUT}=300mA	1.2V≤V_{OUT}<1.5V	--	1.2	1.3	V
			I_{OUT}=300mA	1.5V≤V_{OUT}<1.8V	--	1.1	1.2	
			I_{OUT}=300mA	1.8V≤V_{OUT}<2.5V	--	0.6	0.7	
			I_{OUT}=300mA	2.5V≤V_{OUT}<2.8V	--	0.4	0.5	
			I_{OUT}=300mA	2.8V≤V_{OUT}<3.3V	--	0.36	0.48	
			I_{OUT}=300mA	V_{OUT}≥3.3V	--	0.35	0.45	
Line Regulation		ΔV_{LINE}	V_{IN}=V_{OUT}+1 to 5.5V,I_{OUT}=1mA		--	--	0.17	%/V
Load Regulation		ΔV_{LOAD}	1mA<I_{OUT}<300mA		--	--	2	%/A
Short circuit/start carrying current		I_{SHORT}	R_L=1Ω		--	90	--	mA
EN Leakage Current		I_{EN}	V_{EN}=5.5V		--	--	0.1	μA
Current Limit		I_{LIM}	V_{IN}=5V		--	550	--	mA
EN Input Threshold	Logic Low	V_{IL}	V_{IN}=5V,Shut down		--	--	0.4	V
	Logic High	V_{IH}	V_{IN}=5V,Start up		1.2	--	--	
Output Noise Voltage		e_{NO}	10Hz to100KHz, C_{OUT}=1uF			100	--	μV_{RMS}
Power Supply Rejection Ratio	f=1KHz	PSRR	I_{OUT}=100mA		--	-70	--	dB
	f=10KHz				--	-65	--	
Thermal Shutdown Temperature		T_{SD}	Shutdown, Temp increasing		--	160	--	°C
Thermal Shutdown Hysteresis		T_{SDHY}			--	20	--	°C

Note 1. The dropout voltage is defined as V_{IN} – V_{OUT}, when V_{OUT} is 98% of the normal value of V_{OUT}.

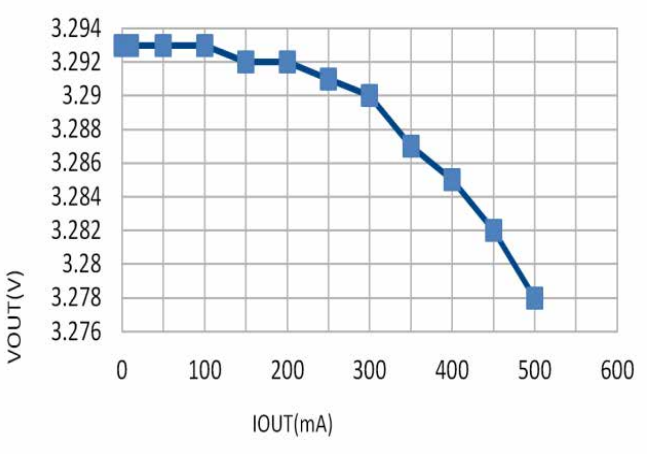
Typical Characteristic Curves



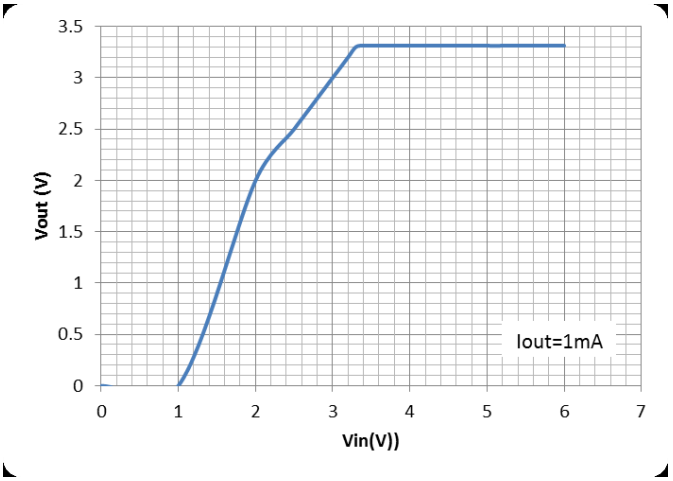
VOUT vs TEMP



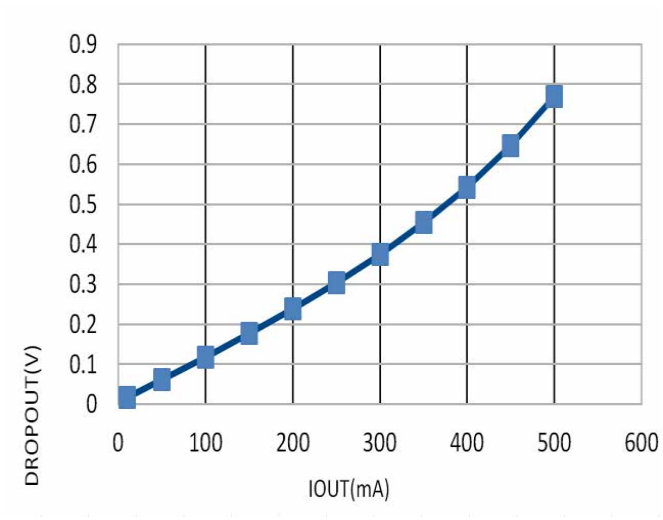
IQ vs VIN



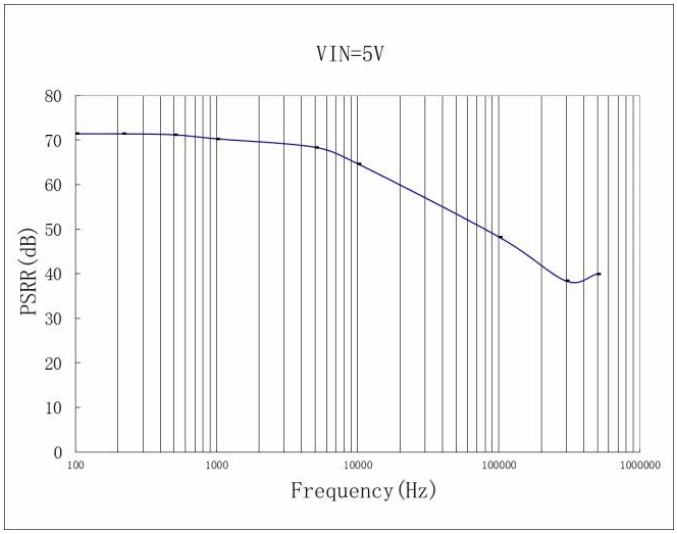
Load Regulation



Line Regulation



Dropout Voltage vs Load Current



PSRR

Applications Information

Input Capacitor

A 1μF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended minimum output capacitance is 1μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to V_{OUT} and GND pins.

Enable Function

The PJ9501 has an EN pin to turn on or turn off the regulator, When the EN pin is in logic high, the regulator will be turned on. The shutdown current is almost 0μA typical. The EN pin may be directly tied to V_{IN} to keep the part on.The Enable input is CMOS logic and cannot be left floating.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula：

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$

Where TJ(MAX) is the maximum operation junction temperature 125 ℃, T_A is the ambient temperature and the $R_{\theta JA}$ is the junction to ambient thermal resistance.

The power dissipation definition in device is：

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

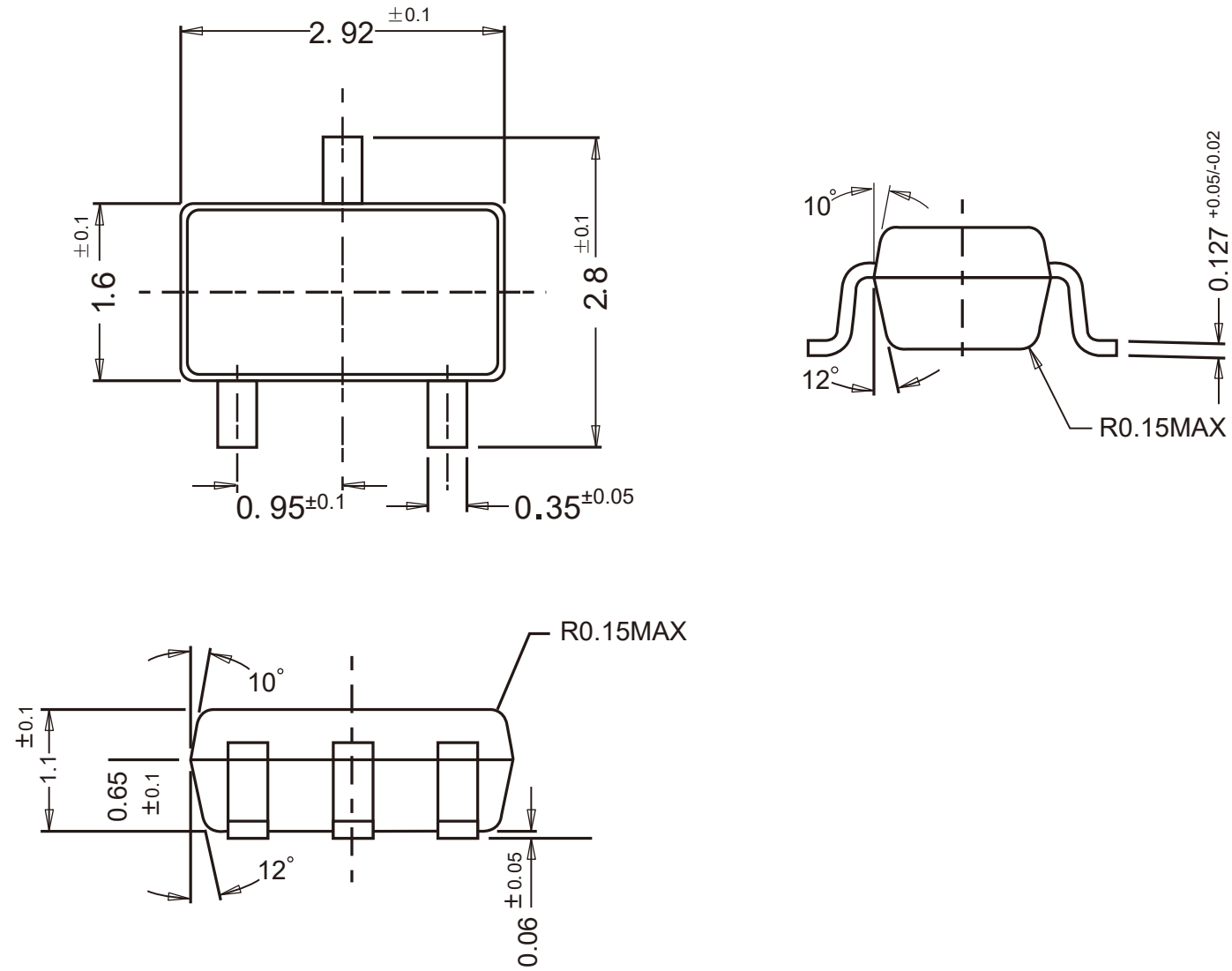
Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the PJ9501 Series ground pin using as wide and as short of a copper trace as is practical.Connections using long trace lengths, narrow trace widths, and connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

Package Outline

SOT-23-3

Dimensions in mm



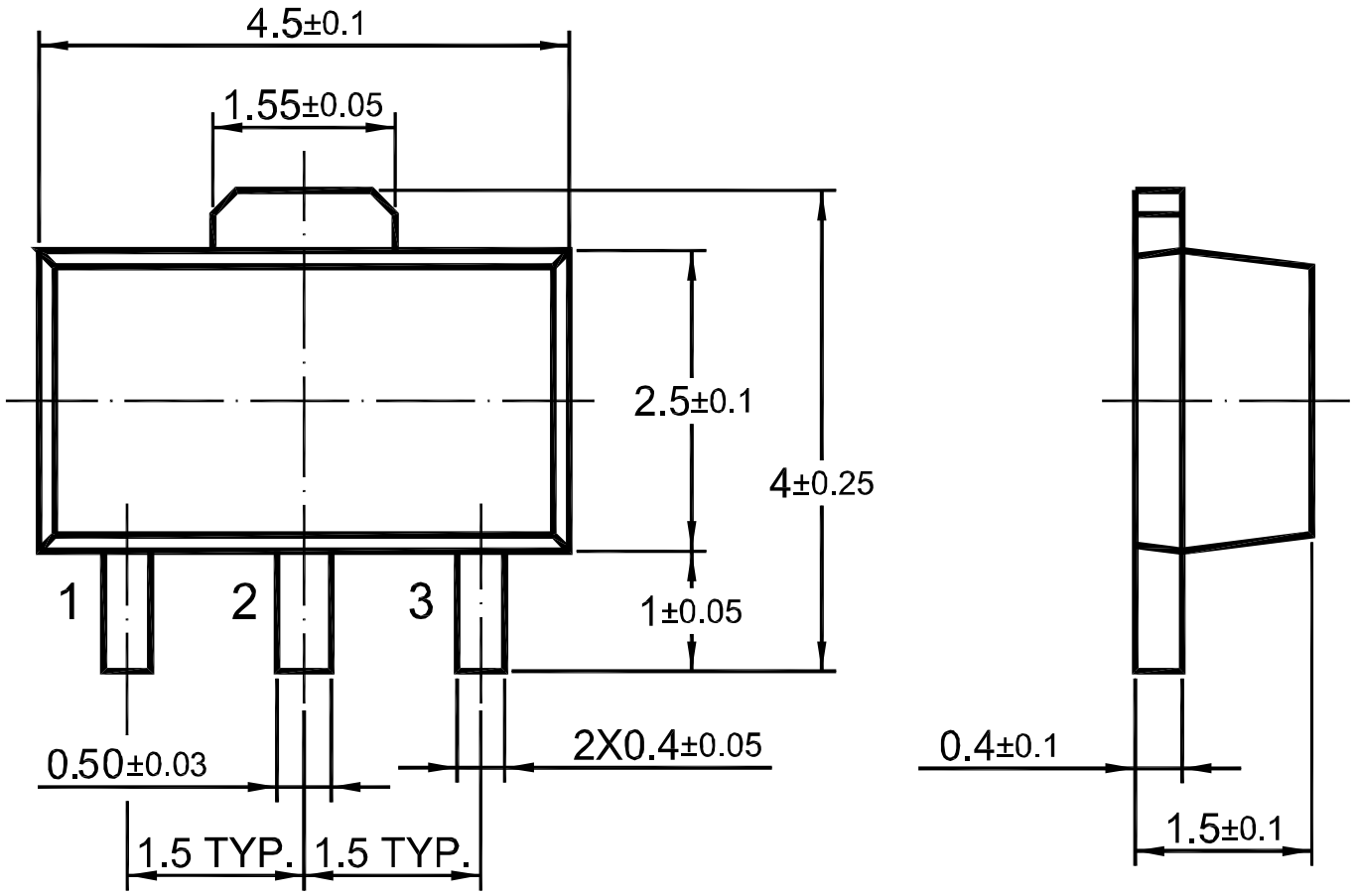
Ordering Information

Device	Package	Shipping
PJ9501 Series	SOT-23-3	3,000PCS/Reel&7inches

Package Outline

SOT-89

Dimensions in mm



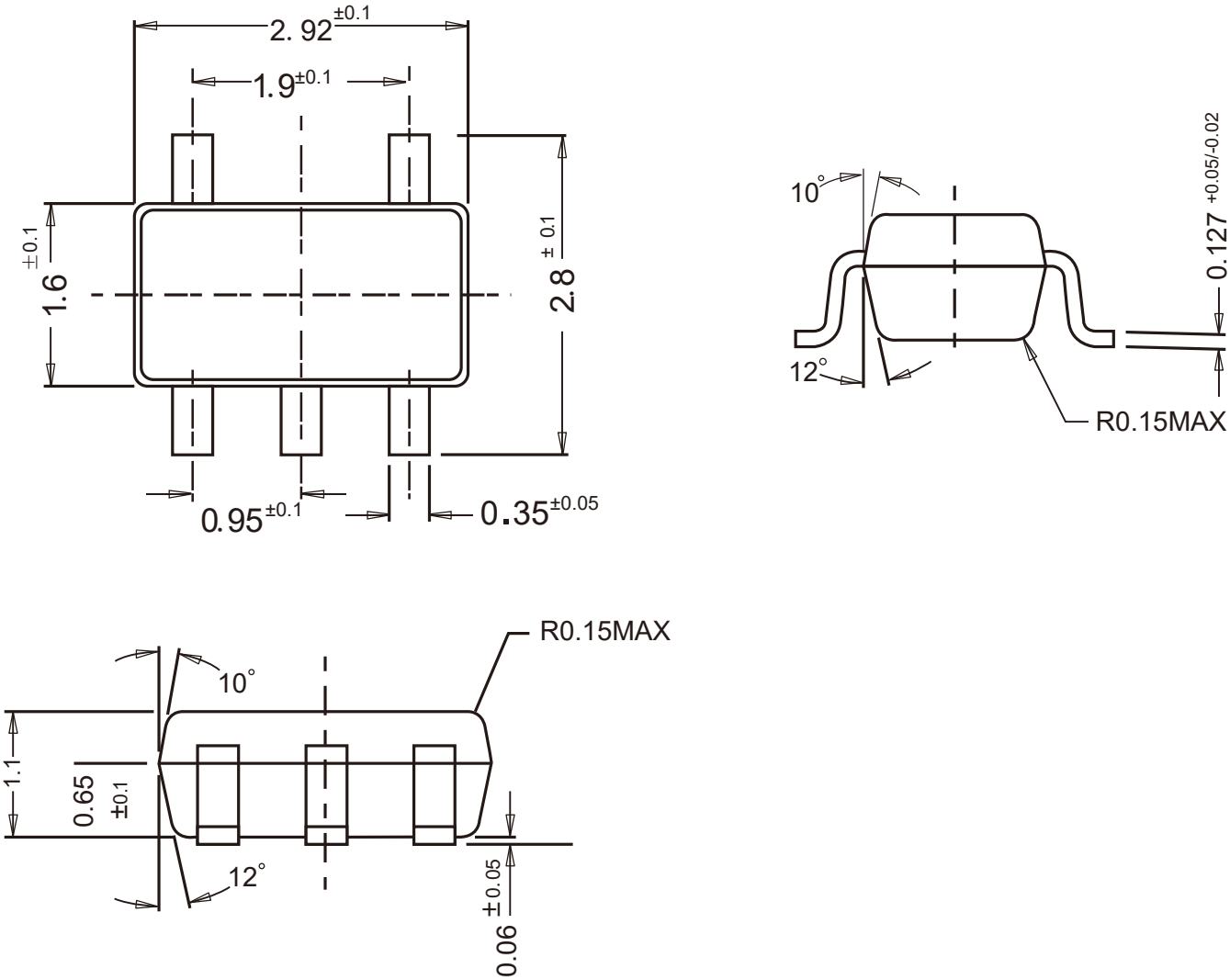
Ordering Information

Device	Package	Shipping
PJ9501 Series	SOT-89	1,000PCS/Reel&7inches
		3,000PCS/Reel&13inches

Package Outline

SOT-23-5

Dimensions in mm

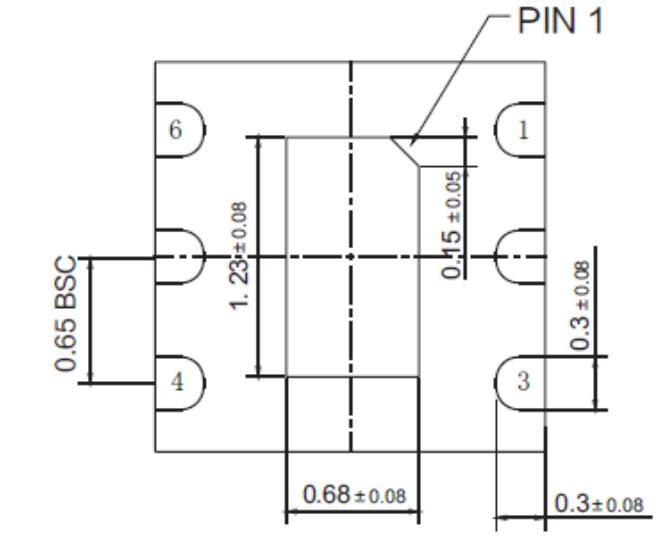


Ordering Information

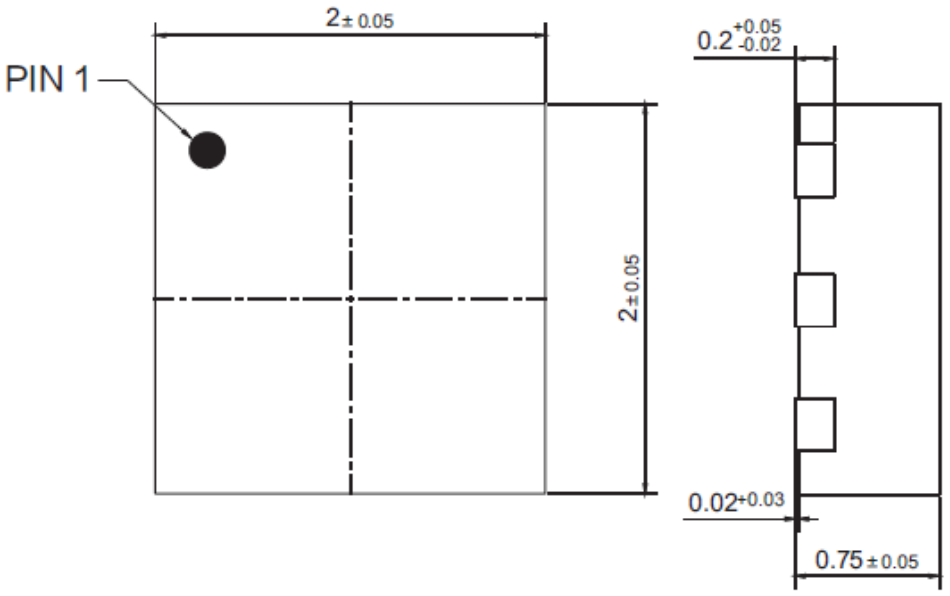
Device	Package	Shipping
PJ9501 Series	SOT-23-5	3,000PCS/Reel&7inches

Package Outline

DFN2x2-6L-0006
Dimensions in mm



BOTTOM VIEW



TOP VIEW SIDE VIEW

Ordering Information

Device	Package	Shipping
PJ9501 Series	DFN2x2C-6L	3,000PCS/Reel&7inches